Climbing the VLSI Power Wall for nm Era

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Low Power, and energy efficiency are key themes which is pushing system, software and hardware design. In order to achieve low power system, circuit and technology co-design is essential. This talk focuses on related technology and important circuit techniques for nanoscale era. Achieving low power and high performance simultaneously is always difficult. Technology has seen major shifts from bulk to SOI and then to non-planar devices such as FinFET/Trigates.

As the technology pushes towards sub-65nm era, process variability and geometric variation in devices can cause variation in power. The reliability also plays an important role in the power-performance envelope. This talk also reviews the methodology to capture such effects and describes all the power components. All the key areas of low power optimization such as reduction in active power, leakage power, and short circuit power are covered. Usage of clock gating, power gating, longer channel, multi-Vt design, stacking, header-footer device techniques, resonant clocking and other methods are described for logic and memory. Finally the talk summarizes key challenges in achieving low power.

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